EE 330
Lecture 3

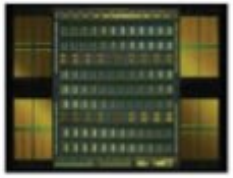
Basic Concepts

- Feature Sizes
- Reliability
- Yield

Review from last lecture:

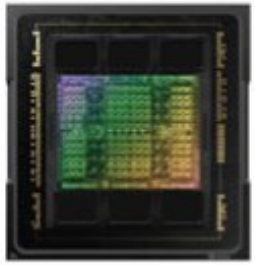
AI Chips

(from Nvidia)

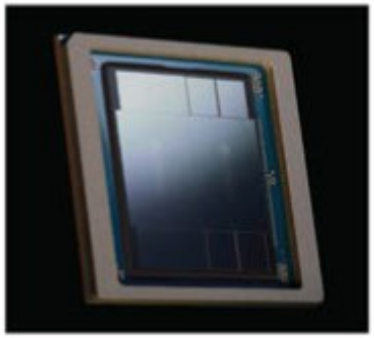


Volta
>21 billion transistors
815mm^2
TSMC 12nm FFN

Ampere
>54 billion transistors
826 mm^2
TSMC N7



Hopper
>80 billion transistors
814 mm^2
TSMC 4N



Blackwell
>208 billion transistors
>1600 mm^2
TSMC 4NP

A New Class of AI Superchip

NVIDIA Blackwell-architecture GPUs pack 208 billion transistors and are manufactured using a custom-built TSMC 4NP process. All NVIDIA Blackwell products feature two reticle-limited dies connected by a 10 terabytes per second (TB/s) chip-to-chip interconnect in a unified single GPU.

Review from last lecture:

Moore's Law

(from Wikipedia)

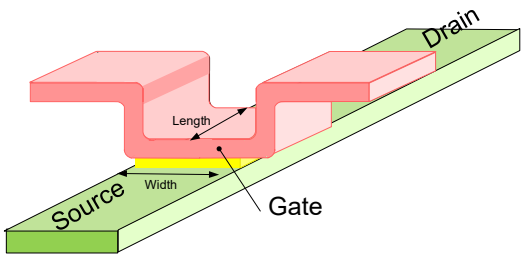
Moore's law is the empirical observation that the complexity of integrated circuits, with respect to minimum component cost, doubles every 24 months[1]. It is attributed to Gordon E. Moore[2], a co-founder of Intel.

- Observation, not a physical law
- Often misinterpreted or generalized
- Many say it has been dead for several years
- Many say it will continue for a long while
- Not intended to be a long-term prophecy about trends in the semiconductor field
- Something a reporter can always comment about when they have nothing to say!

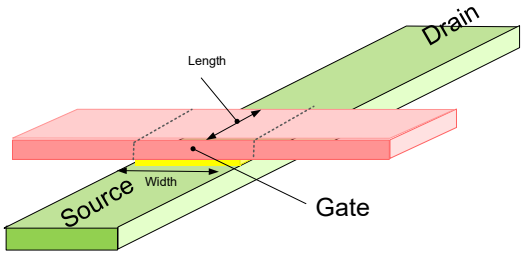
Device scaling, device count, circuit complexity, device cost, … in leading-edge processes will continue to dramatically improve (probably nearly geometrically with a time constant of around 2 years) for the foreseeable future !!

Review from last lecture:

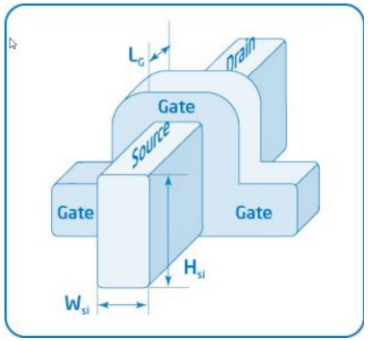
Field Effect Transistors



Planar
MOSFET
(LOCOS)



Planar
MOSFET
(STI)



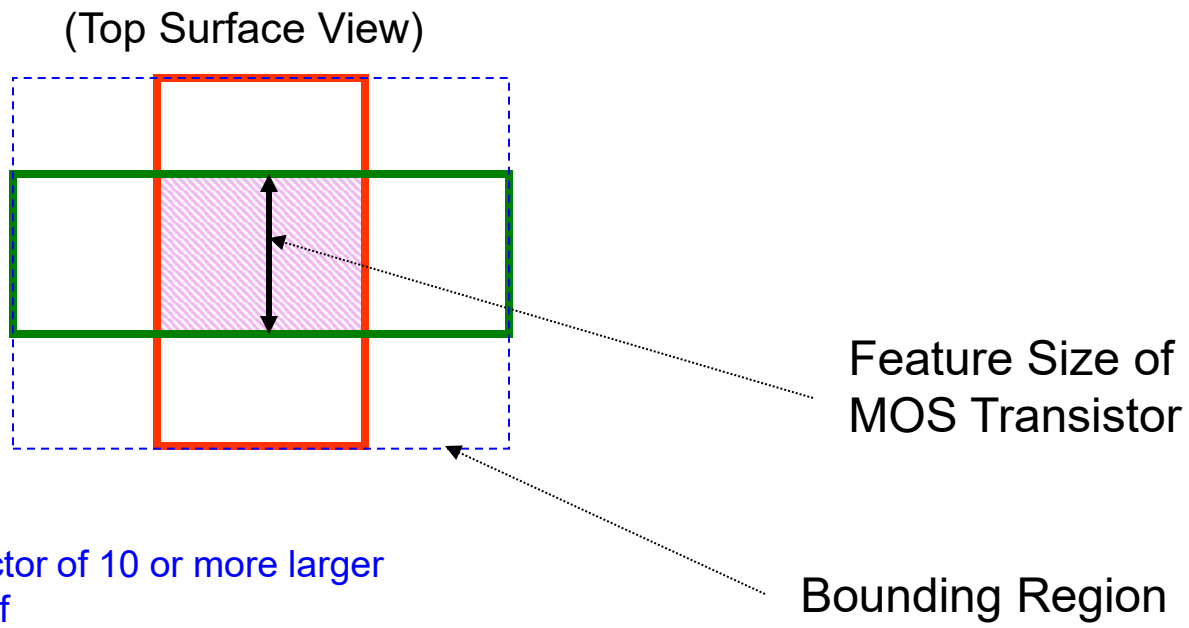
FinFET
Tri-Gate

Dielectric not shown

Review from last lecture:

Feature Size

The feature size of a process generally corresponds to the minimum lateral dimensions of the transistors that can be fabricated in the process



- Bounding region often a factor of 10 or more larger than area of transistor itself
- This along with interconnect requirements and sizing requirements throughout the circuit create an area overhead factor of 10x to 100x

Review from last lecture:

Essentially All Activities Driven by Economic Considerations

- Many Designs Cost Tens of Millions of Dollars
- Mask Set and Production of New Circuit Approaching $2 Million
- New Foundries Costs Approaching $10 Billion (few players in World can compete)
- Many Companies Now Contract Fabrication (Fabless Semiconductor Companies)
- Time to Market is Usually Critical
- Single Design Error Often Causes Months of Delay and Requires New Mask Set
- Potential Rewards in Semiconductor Industry are Very High

Will emphasize economic considerations throughout this course

Review from last lecture:

Single Errors Usually Cause Circuit Failure

- How may components were typical of lab experiments in EE 201 and EE 230?
- Has anyone ever made an error in the laboratory of these courses ? (wrong circuit, incomplete understanding, wrong wiring, wrong component values, imprecise communication, frustration …..)
- How many errors are made in a typical laboratory experiment in these courses?
- How many errors per hour might have occurred?

Review from last lecture:

Single Errors Usually Cause Circuit Failure

Consider an extremely complicated circuit

- with requirements to do things that have never been done before
- with devices that are not completely understood
- that requires several billion transistors
- that requires 200 or more engineers working on a project full-time for 3 years
- with a company investment of many million dollars
- with an expectation that nobody makes a single error

Is this a challenging problem for all involved?

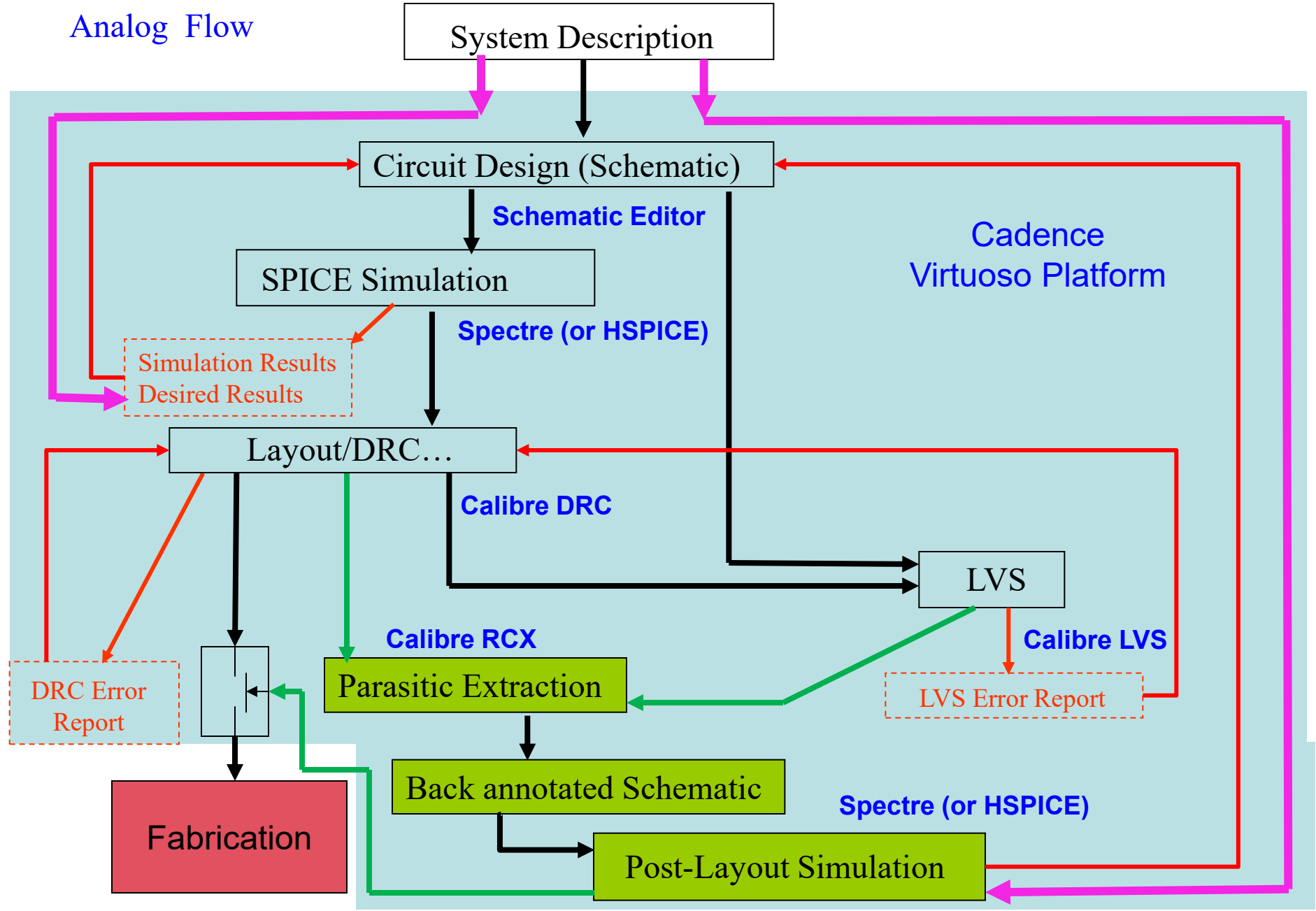
Review from last lecture:

How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

- CAD tools and CAD-tool environment critical for success today
- Small number of VLSI CAD toolset vendors
- CAD toolset helps the engineer and it is highly unlikely the CAD tools will replace the design engineer
- An emphasis in this course is placed on using toolset to support the design process

Review from last lecture:

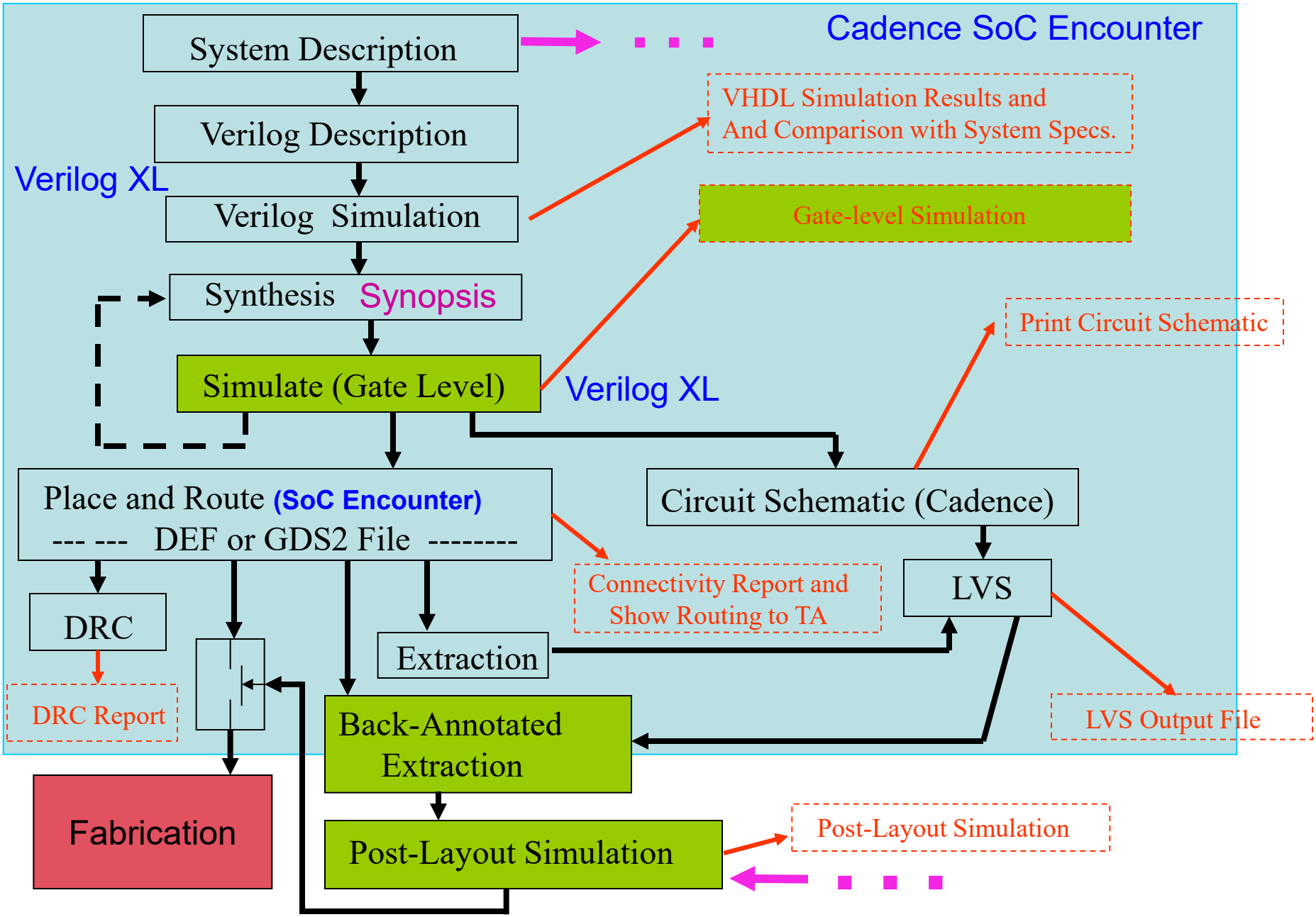
VLSI Design Flow Summary



Review from last lecture:

Digital Flow

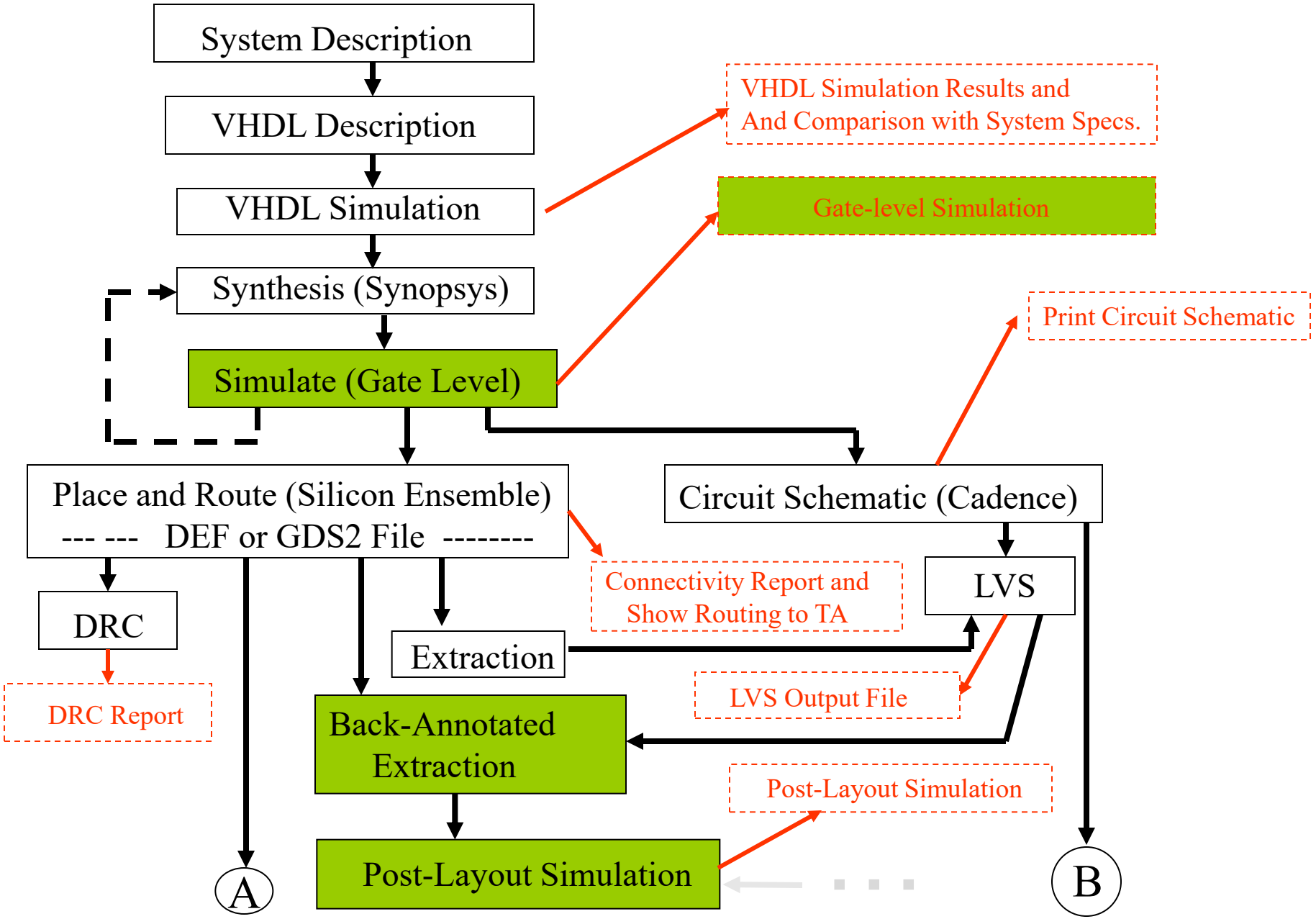
VLSI Design Flow Summary



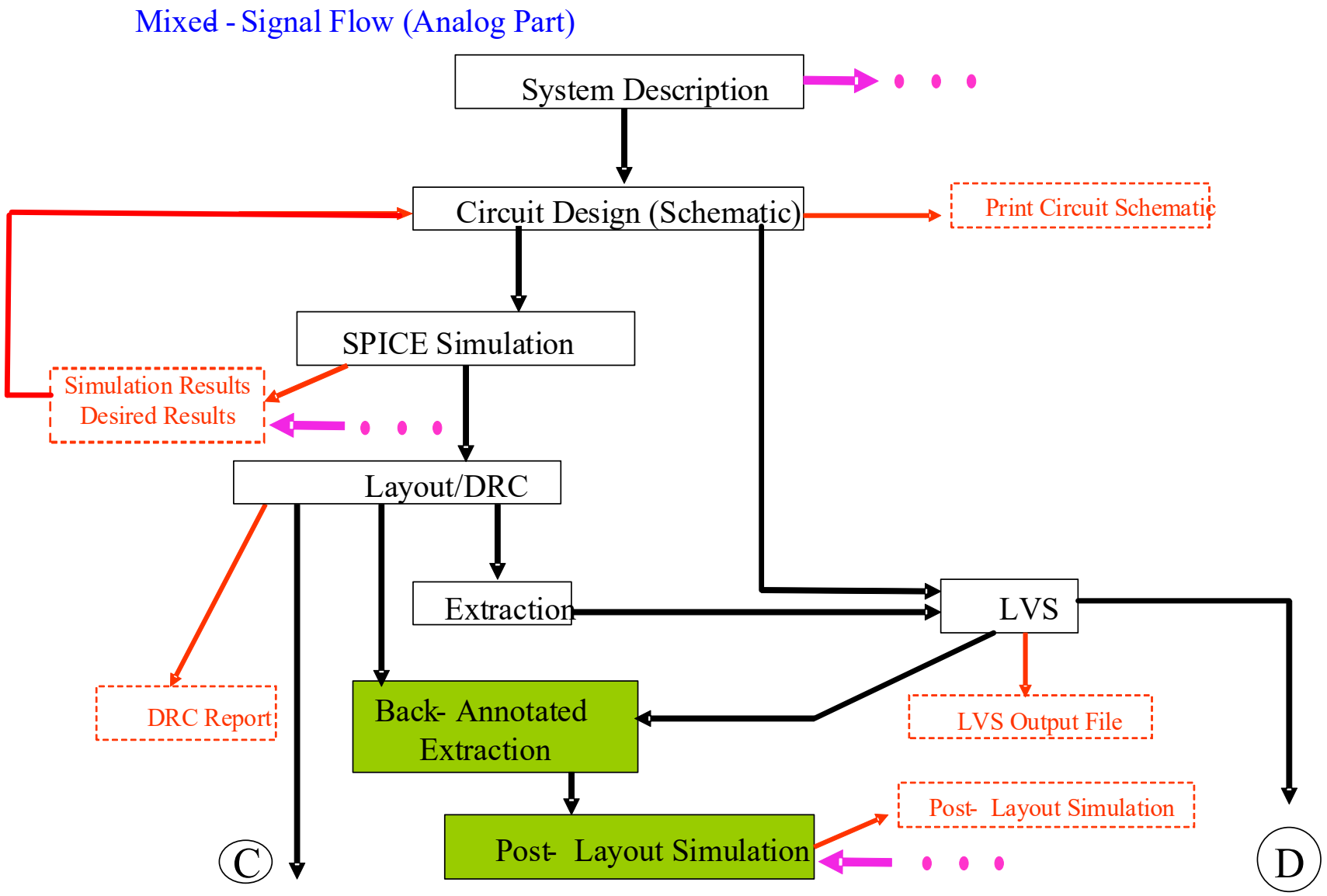
Review from last lecture:

VLSI Design Flow Summary

Mixed Signal Flow (Digital Part)



Review from last lecture: **VLSI Design Flow Summary**

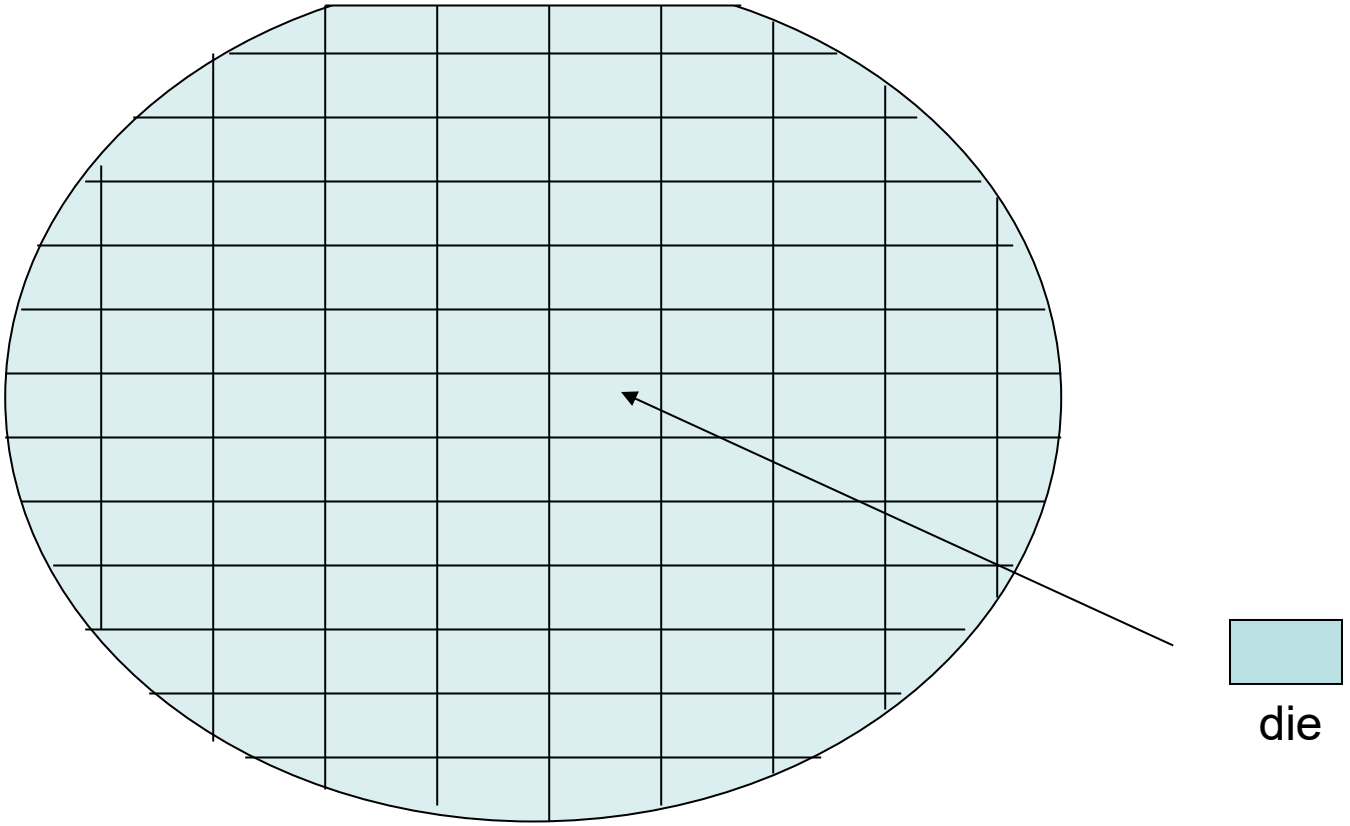


Review from last lecture:

Comments

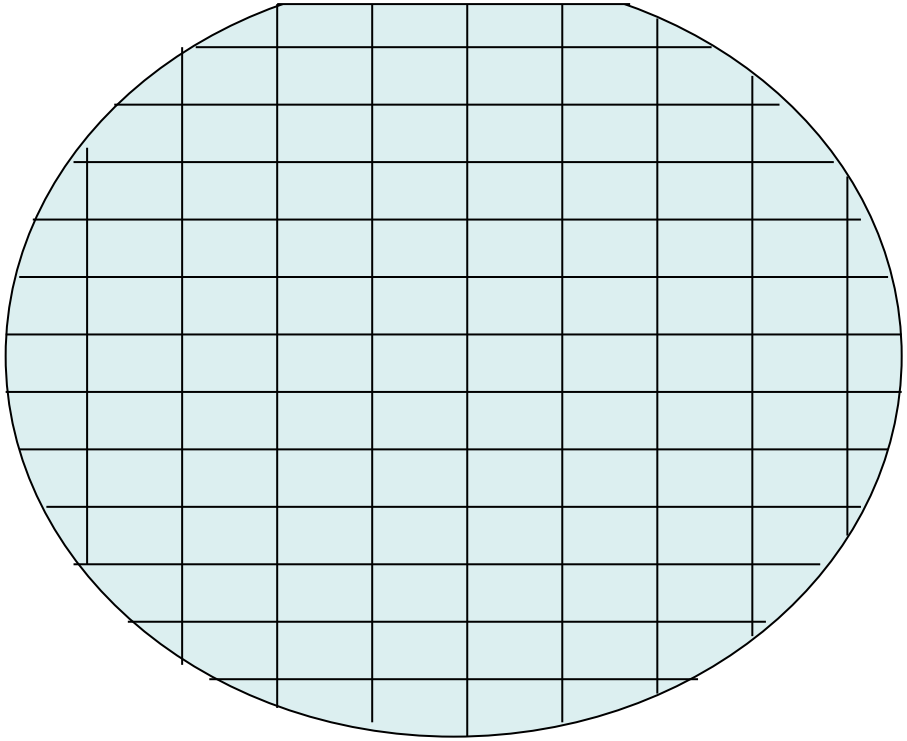
- The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems
- Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits

Wafer



- 6 inches to 18 inches in diameter (300mm/12 inch most common, 450nm likely won't happen)
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small

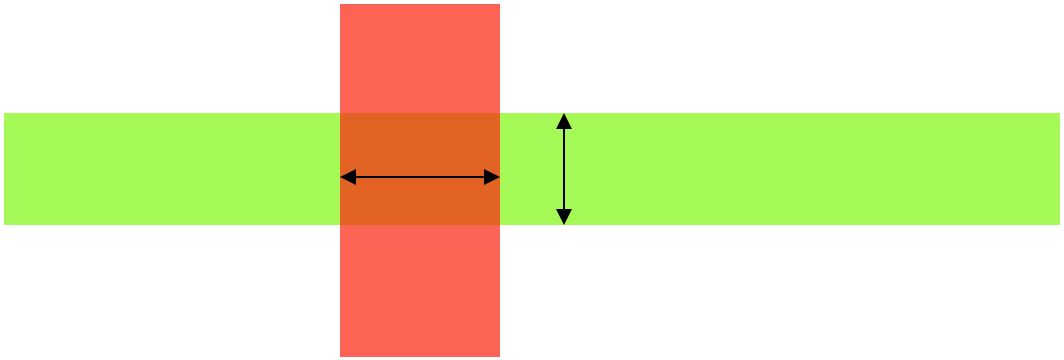
Why are wafers round?



- Ingot spins (rotates) as crystal is being made (dominant reason)
- Edge loss would be larger with rectangular wafers
- Heat is more uniformly distributed during processing
- Size of furnace is smaller for round wafers
- Wafers are spun during application of photoresist and even coatings is critical
- Optics for projection are better near center of image

Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured



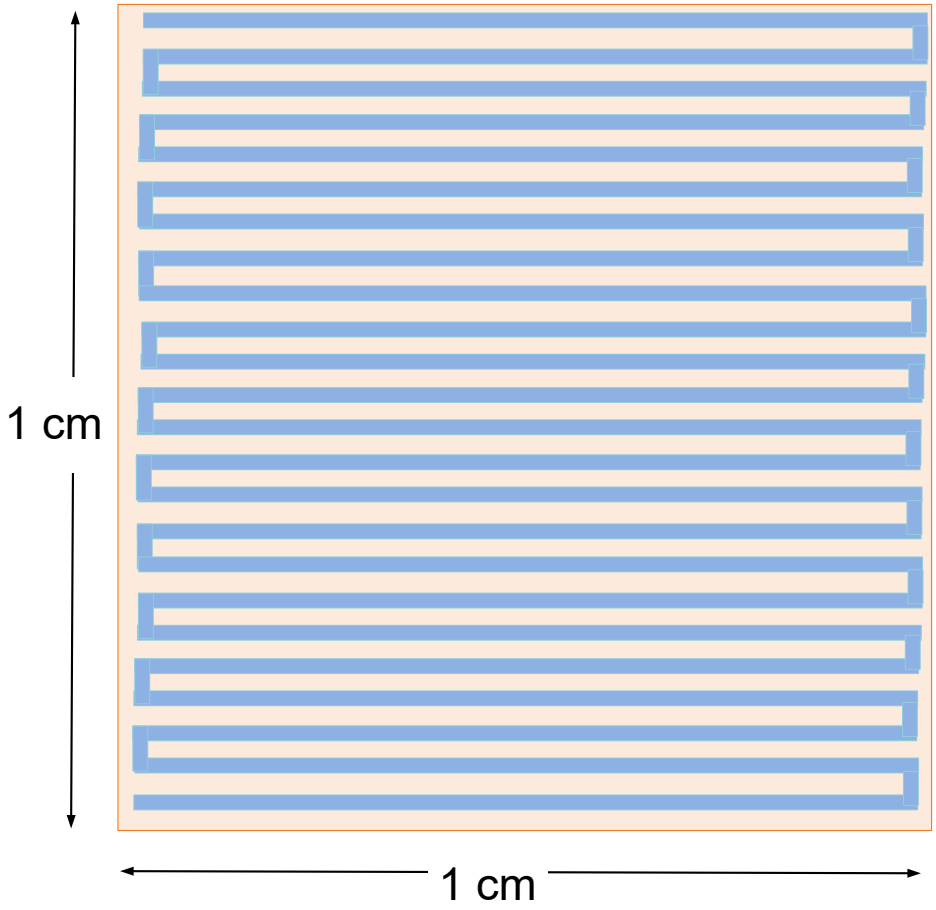
Often given as either feature size or pitch

Minimum feature size often identical for different features

Extremely challenging to decrease minimum feature size in a new process

Reliability

Consider the following example:



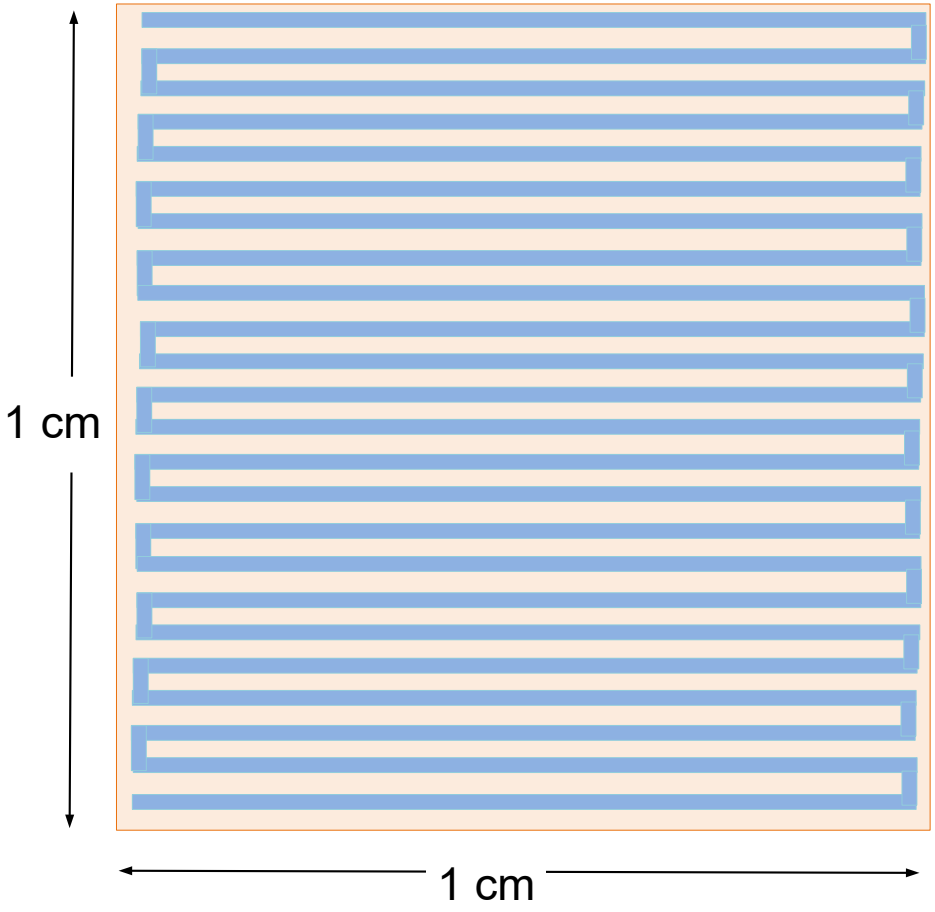
Assume:

- Die contains only interconnect
- Area 1cm^2
- 5nm process (10nm pitch)
- 10 levels of interconnect (actually pitch will increase in higher levels but ignore that)

How long is the total interconnect?

Reliability

How long is the total interconnect?



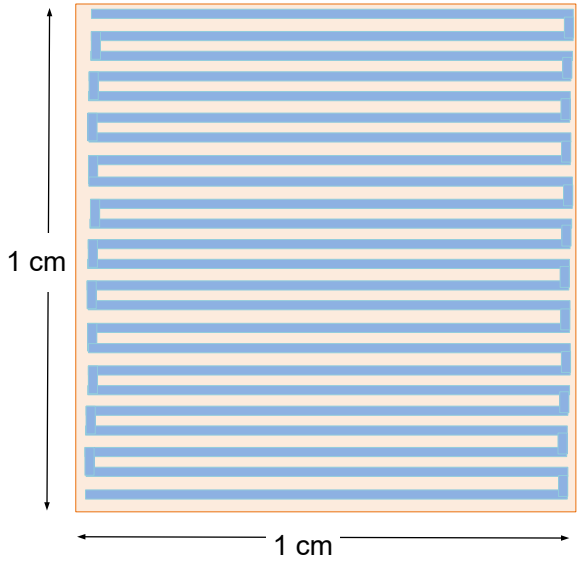
n=number of stripes:

$$n = \frac{1cm}{5nm + 5nm} = \frac{10^{-2}}{10x10^{-9}} = 10^{6}$$

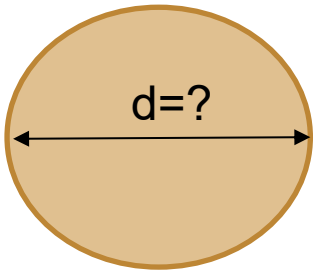
$$L = n_{LEVELS} \bullet L_{LEVEL} = 10 \bullet 10^{6}\, x1cm = 100km$$

$$L = 62 \ \ miles$$

Reliability



In perspective:



Human Hair

5nm

How do these dimensions compare to that of the human hair?

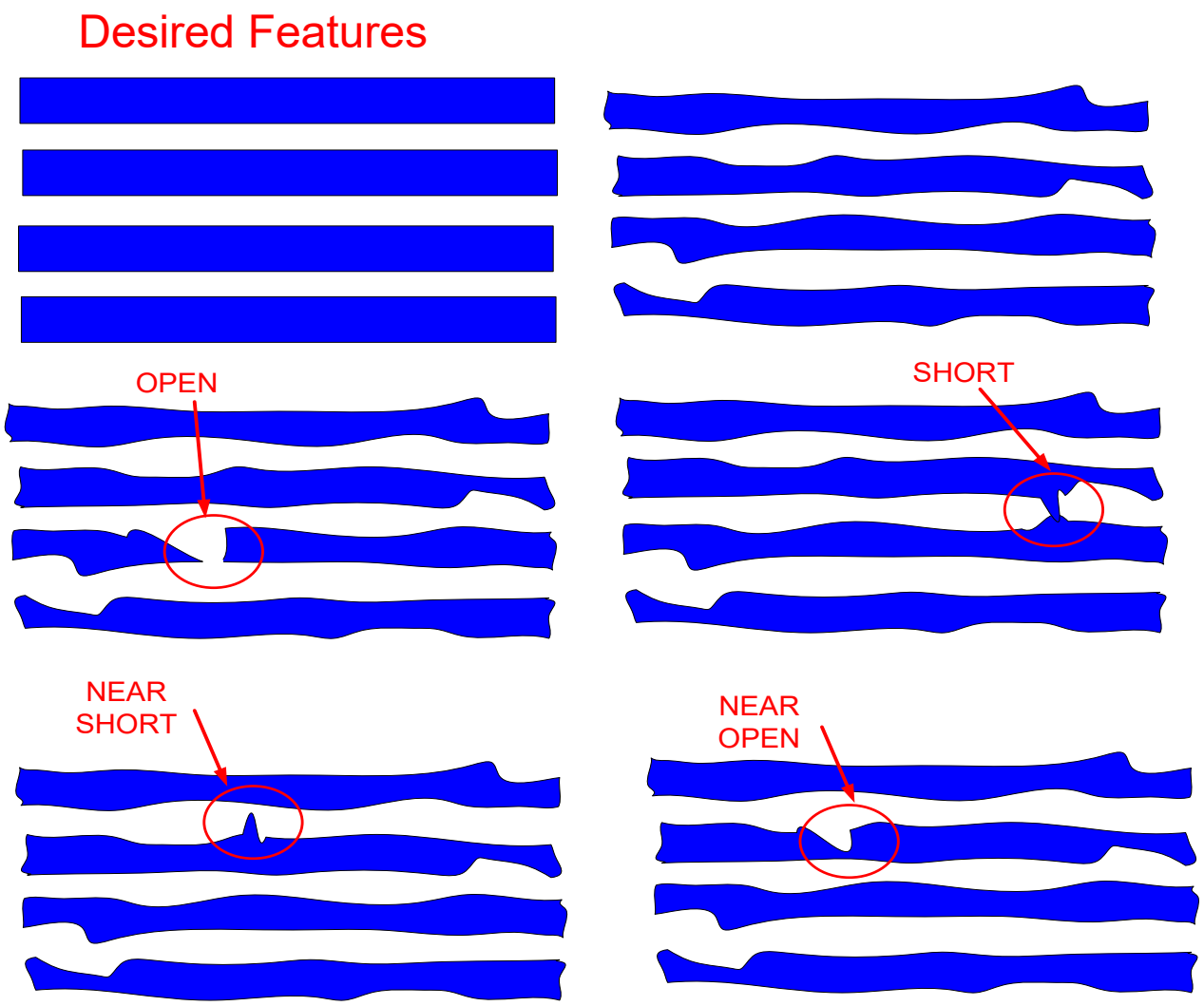
Human Hair Diameter: 18um to 180um

Assume d=50um

$$r = \frac{d}{5nm} = \frac{50um}{5nm} = 10{,}000$$

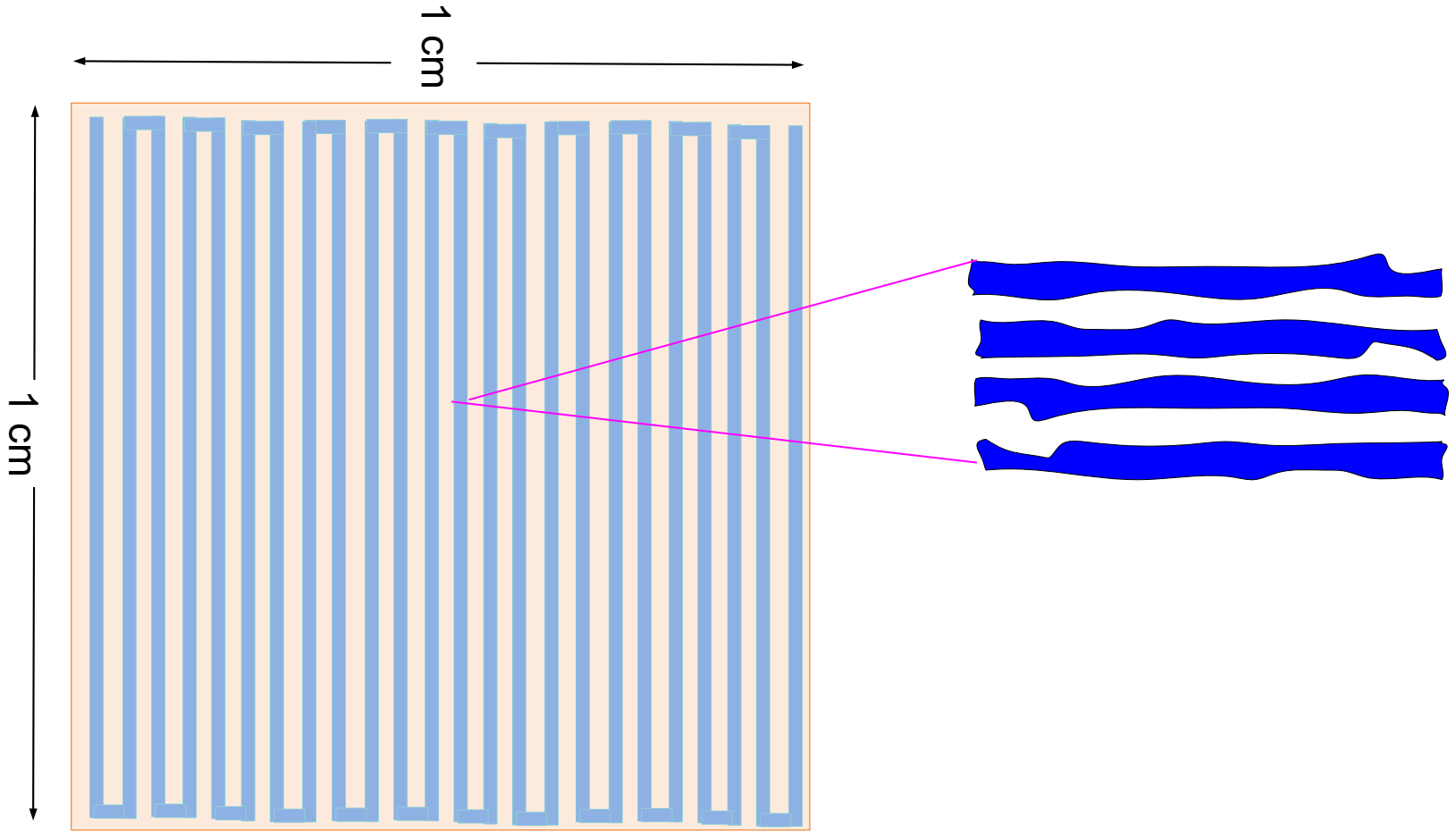
- Length of 5nm transistor 10,000 times smaller than the diameter of a 50um hair
- If interconnect were square (not quite) cross-sectional area would be 100 million times smaller !

Reliability Problems



Actual features show some variability (dramatically exaggerated here !!!!)

Reliability Challenges



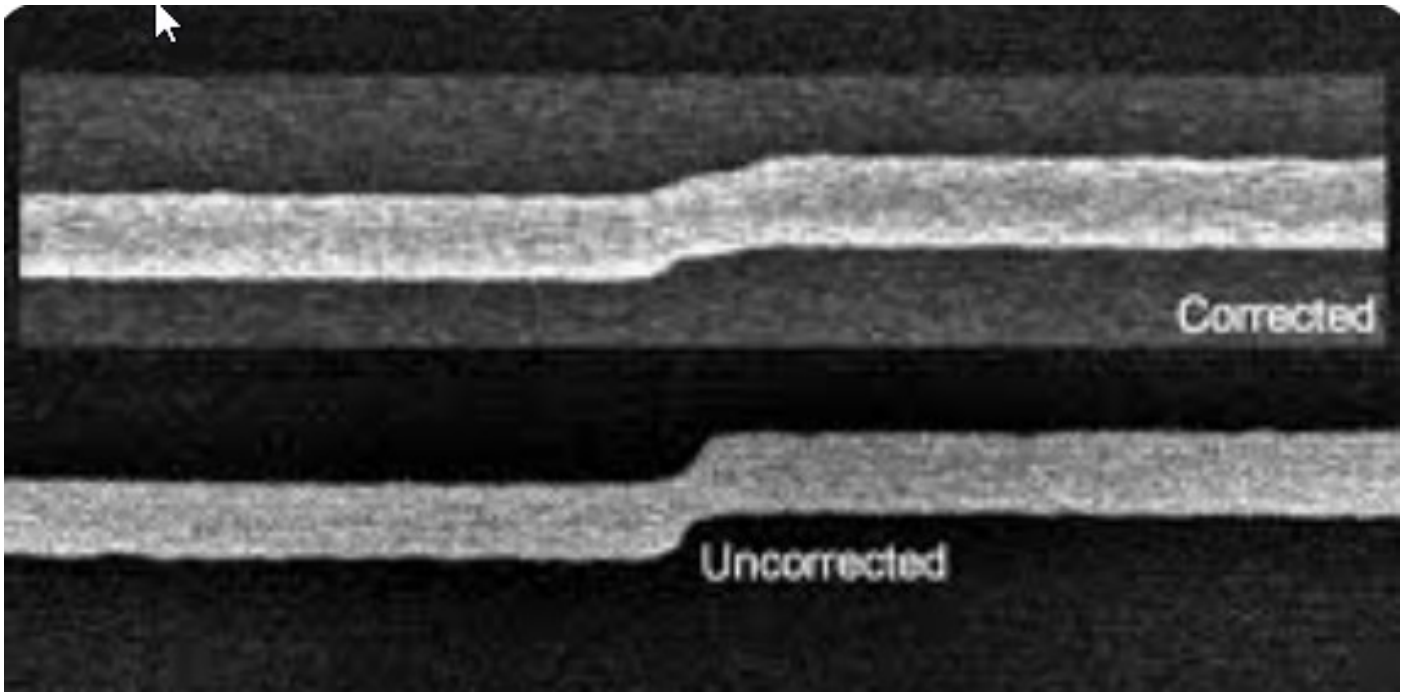
Can not tolerate one defect in 62 miles in these interconnects that are 5nm wide

Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured

Feature size is specified so that there is a very low probability of a single processing defect occurring any place on a die !

SEM Images of Irregularity and/or Defects



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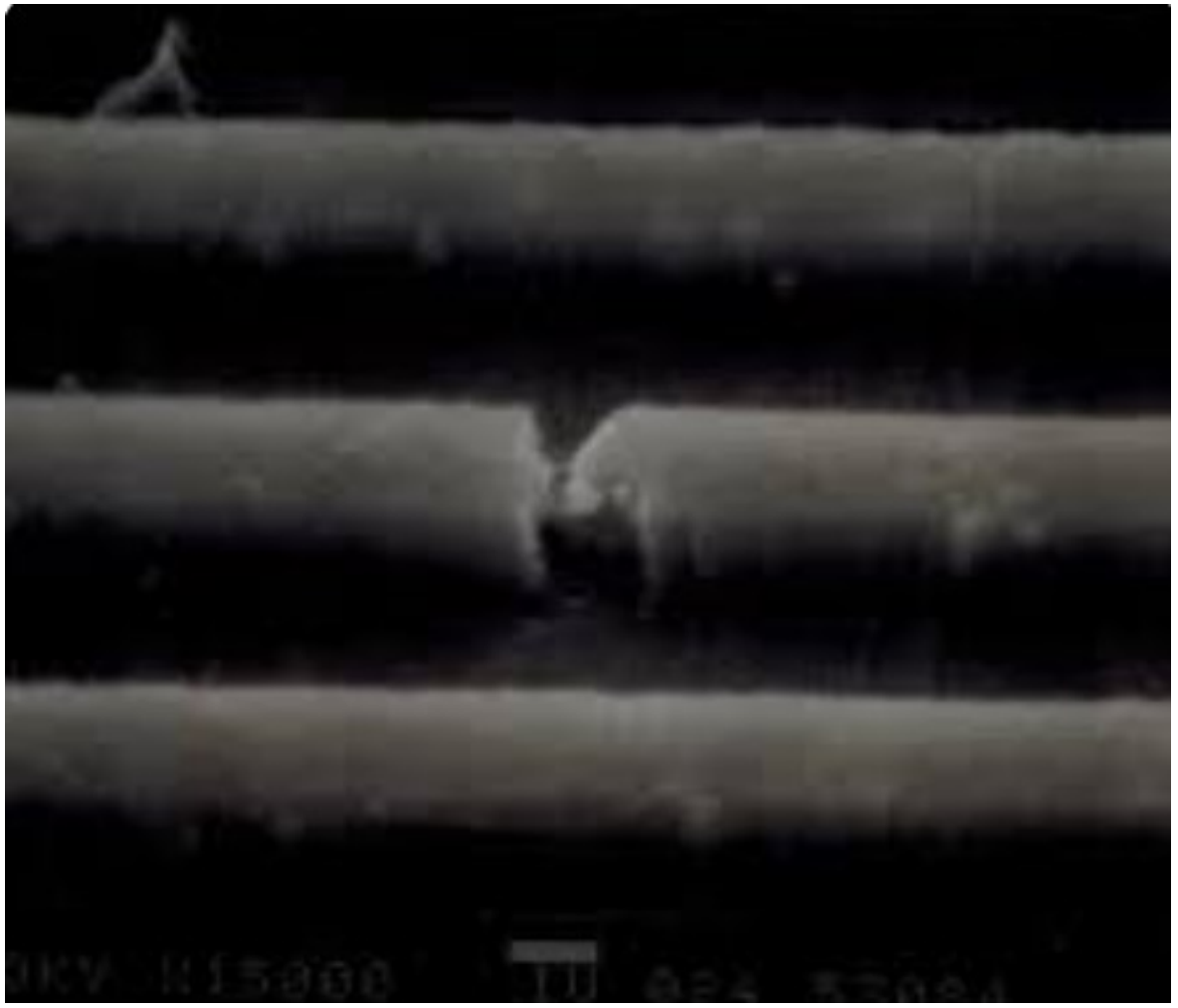

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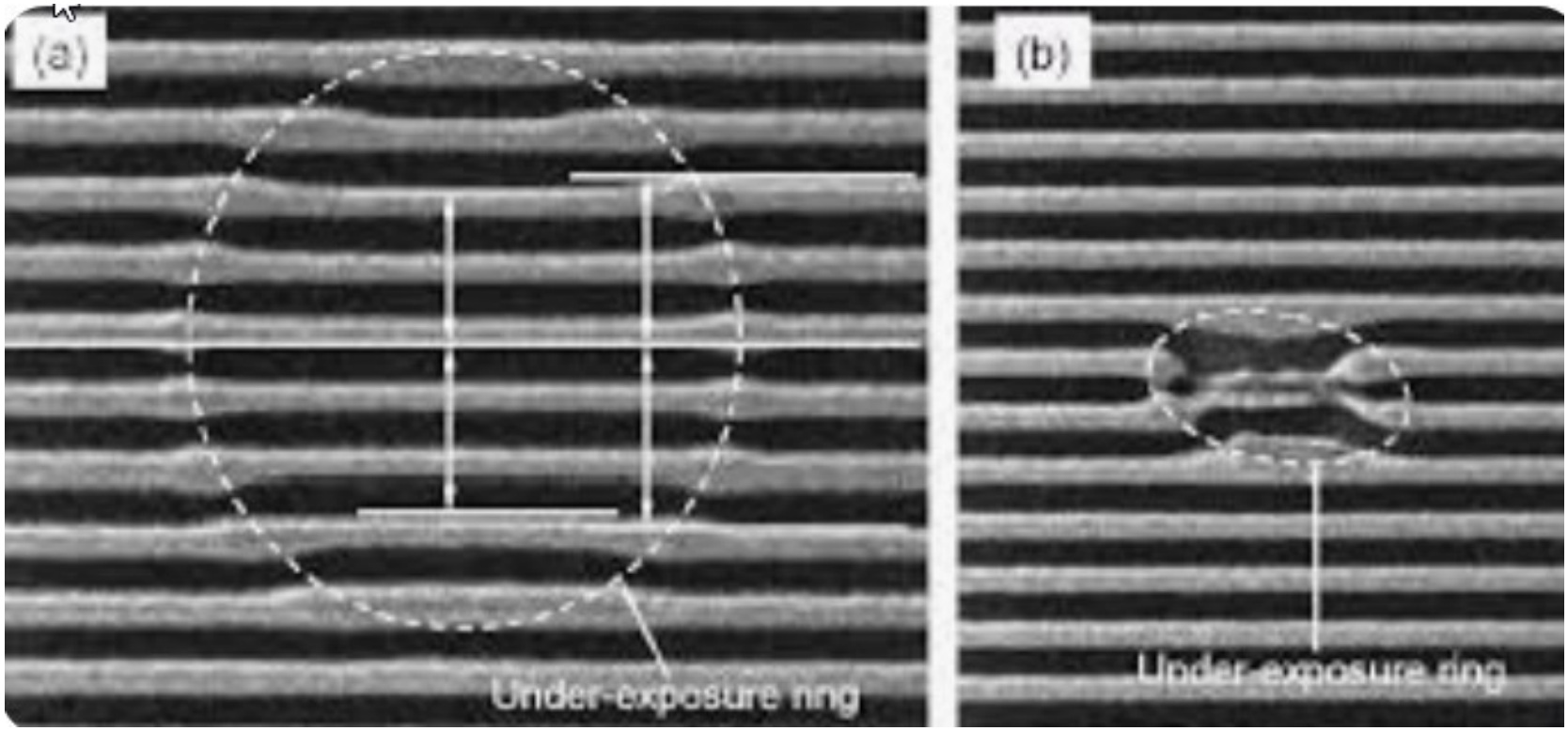

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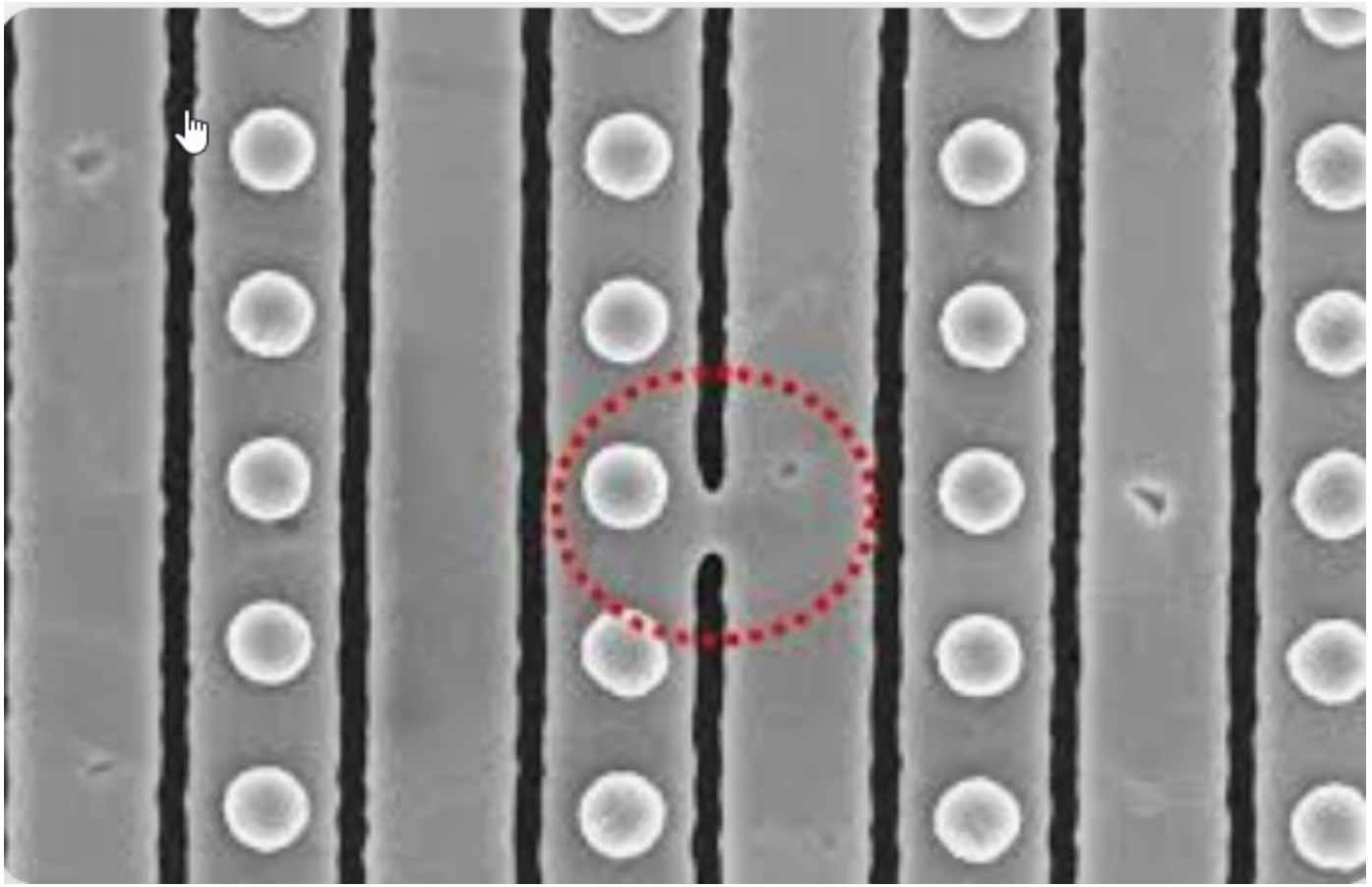

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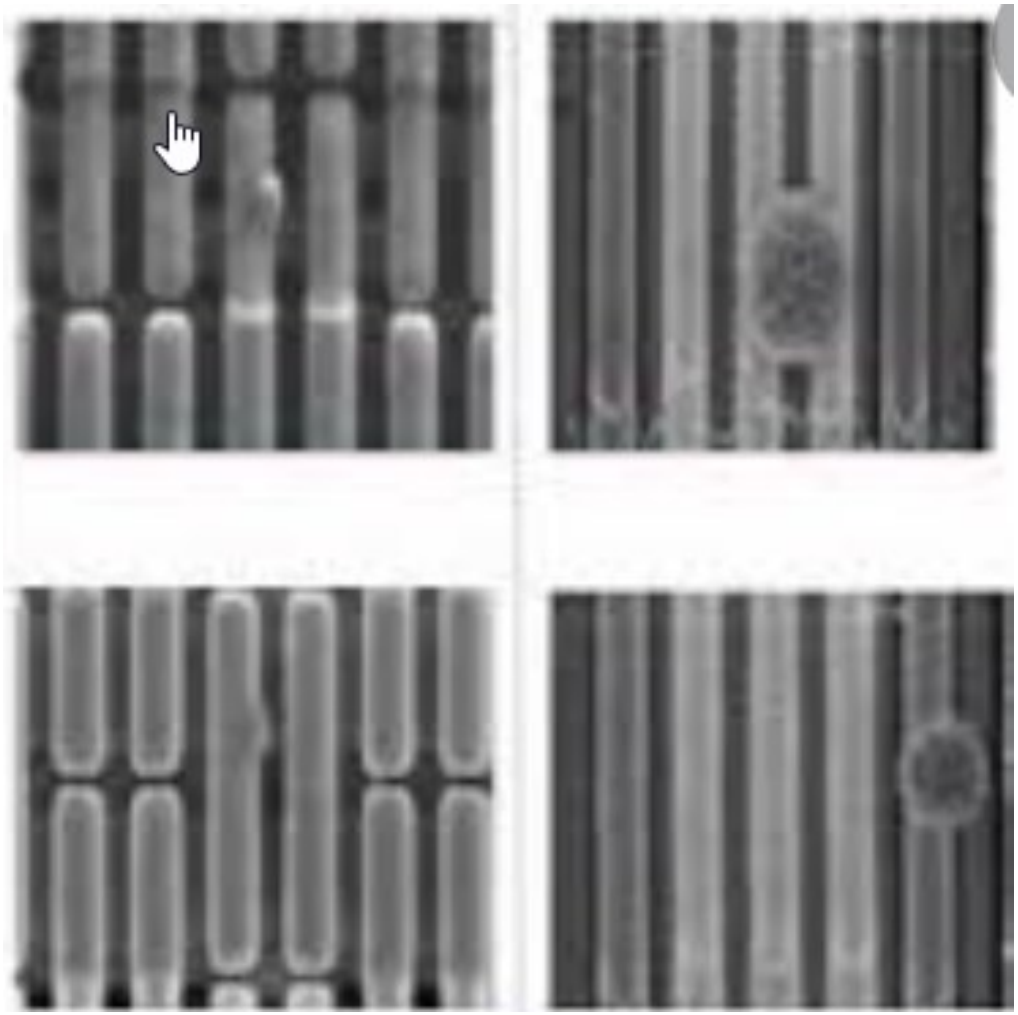

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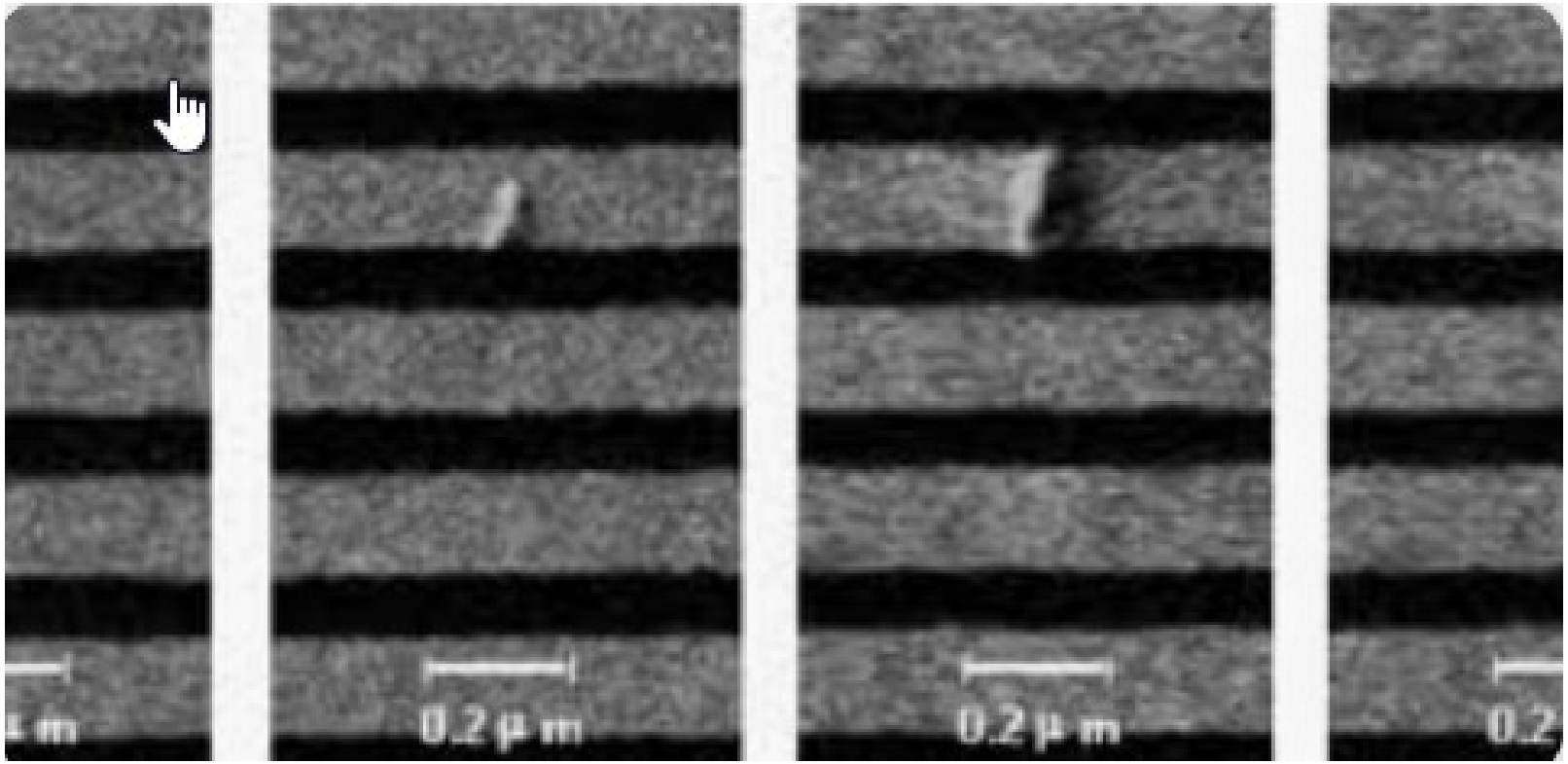

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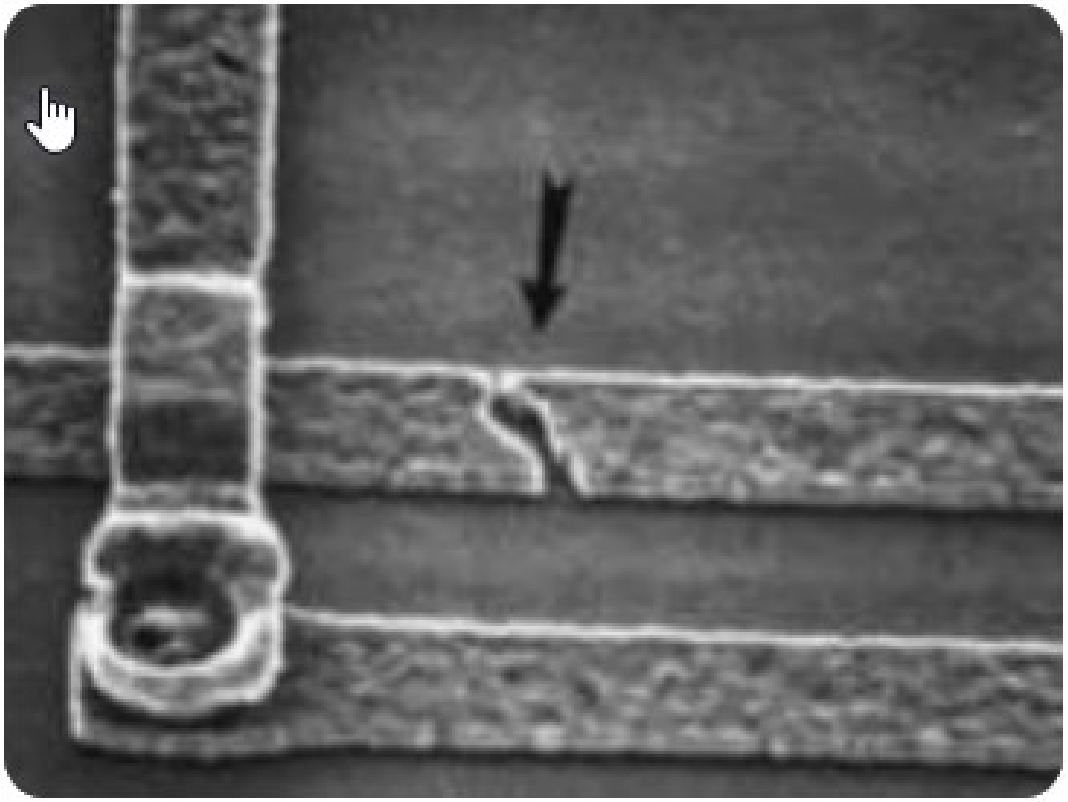


Semiconductor Electromigration In...

Copper can support approximately 5 times the current density as aluminum at a given electromigration rate

What is meant by “reliably”

Yield is acceptable if circuit performs as designed even when a very large number of these features are made

If P is the probability that a feature is good

n is the number of uncorrelated features on an IC

Y is the yield

$$Y = P^n$$

$$P = e^{\frac{\log_e Y}{n}}$$

Example: How reliable must a feature be?

n=5E3

Y=0.9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}}$$ **=0.999979**

But is n=5000 large enough ? is Y large enough?

More realistically n=5E9 (or even 5E10 or even 5E11)

Consider n=5E9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E9}}$$ **=0.999999999979**

20 parts in a trillion or size of a piece of sheetrock relative to area of Iowa

Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes

Feature Size

- Typically minimum length of a transistor
- Often also minimum width or spacing of a metal interconnect (wire)
- Point of “bragging” by foundries
  - Drawn length and actual length differ
- Often specified in terms of pitch
  - Pitch is sum of feature size and spacing of same feature
  - Pitch approximately equal to twice minimum feature size

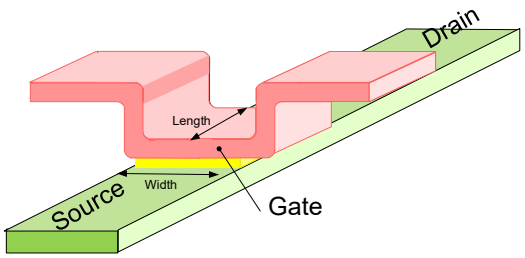
Feature Size Evolution

Mid 70's	25μ
2005	90nm
2010	20nm
2020	7nm
2026	1.8nm ?

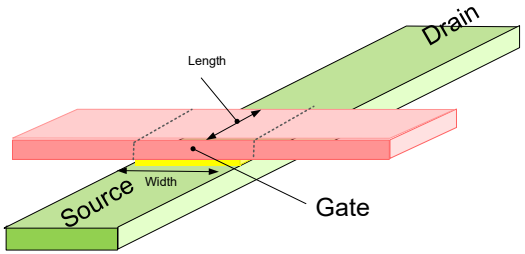
$$1\mu = 10^3\, nm = 10^{-6}\, m = 10^4\ \mathring{\mathrm{A}}$$

Review from last lecture:

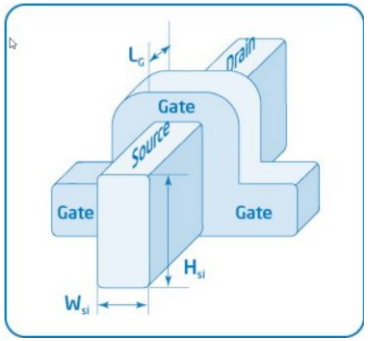
Field Effect Transistors



Planar
MOSFET
(LOCOS)



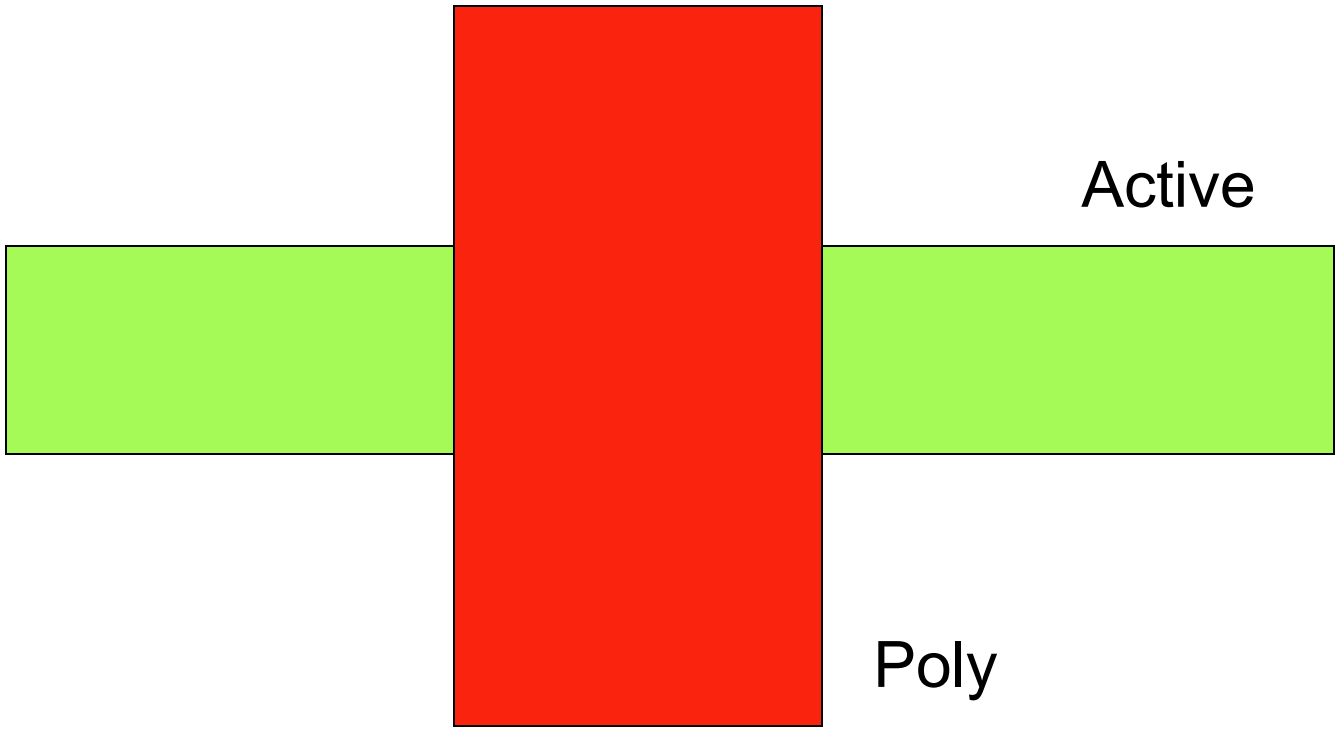
Planar
MOSFET
(STI)



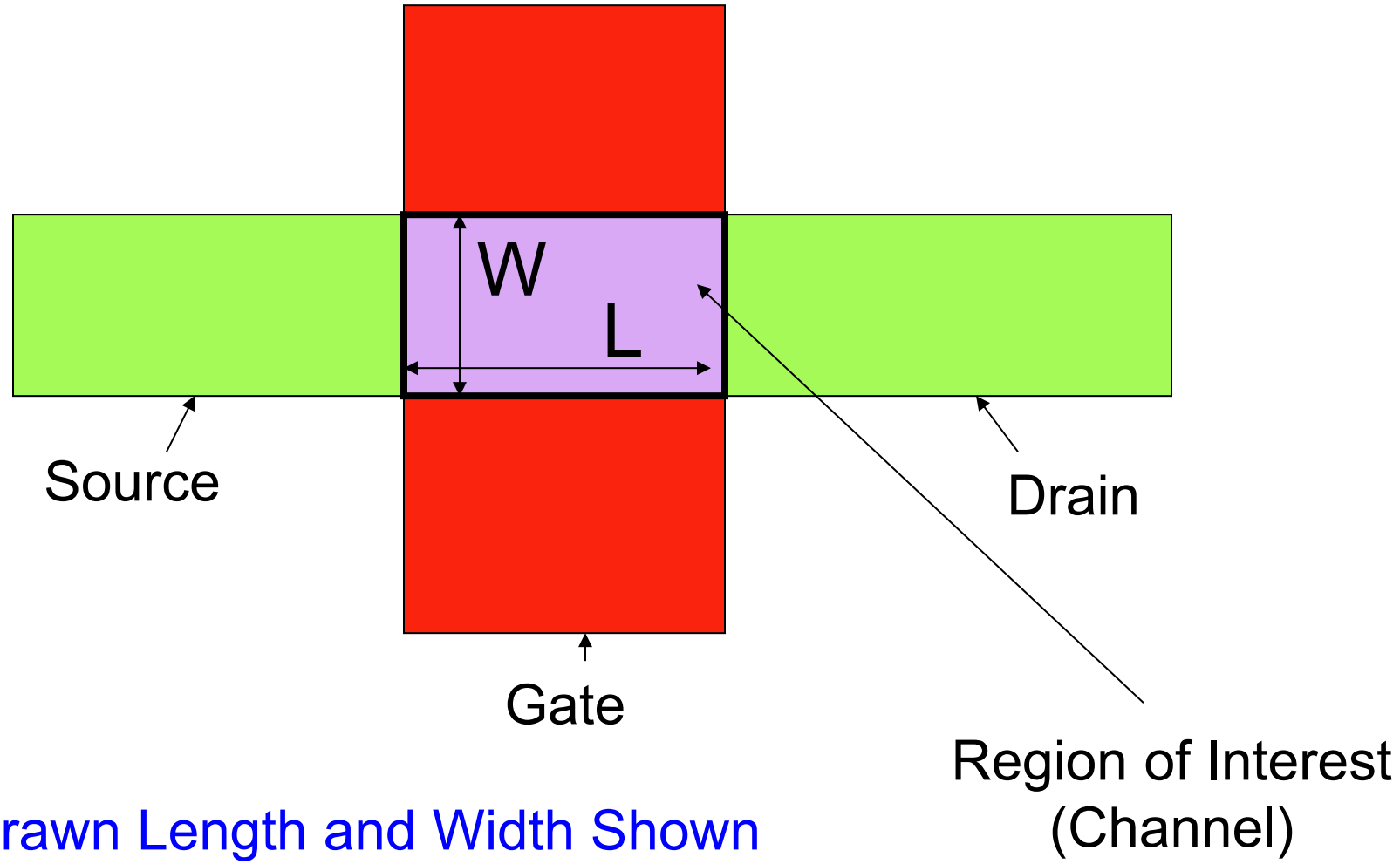
FinFET
Tri-Gate

Dielectric not shown

Planar MOS Transistor



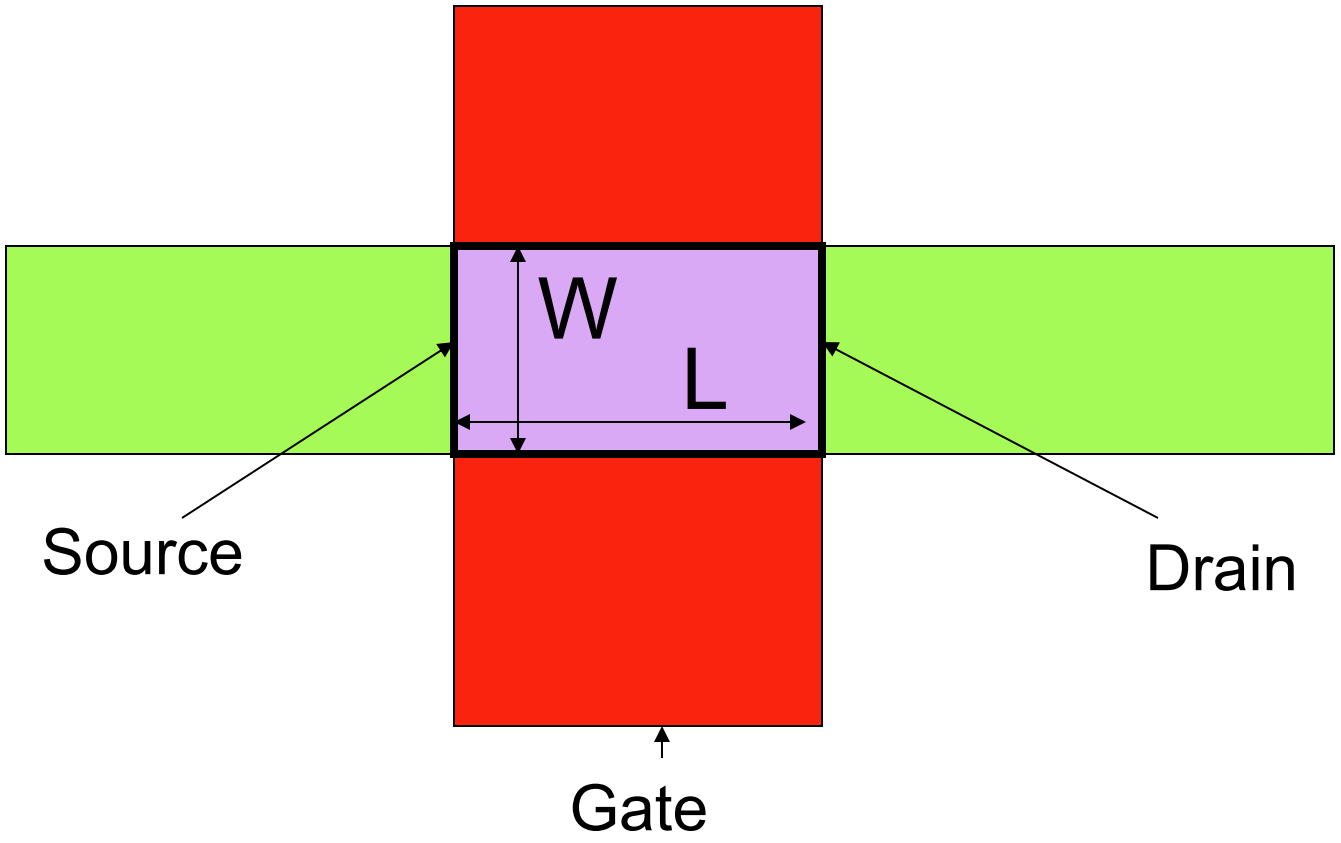
Planar MOS Transistor



Drawn Length and Width Shown

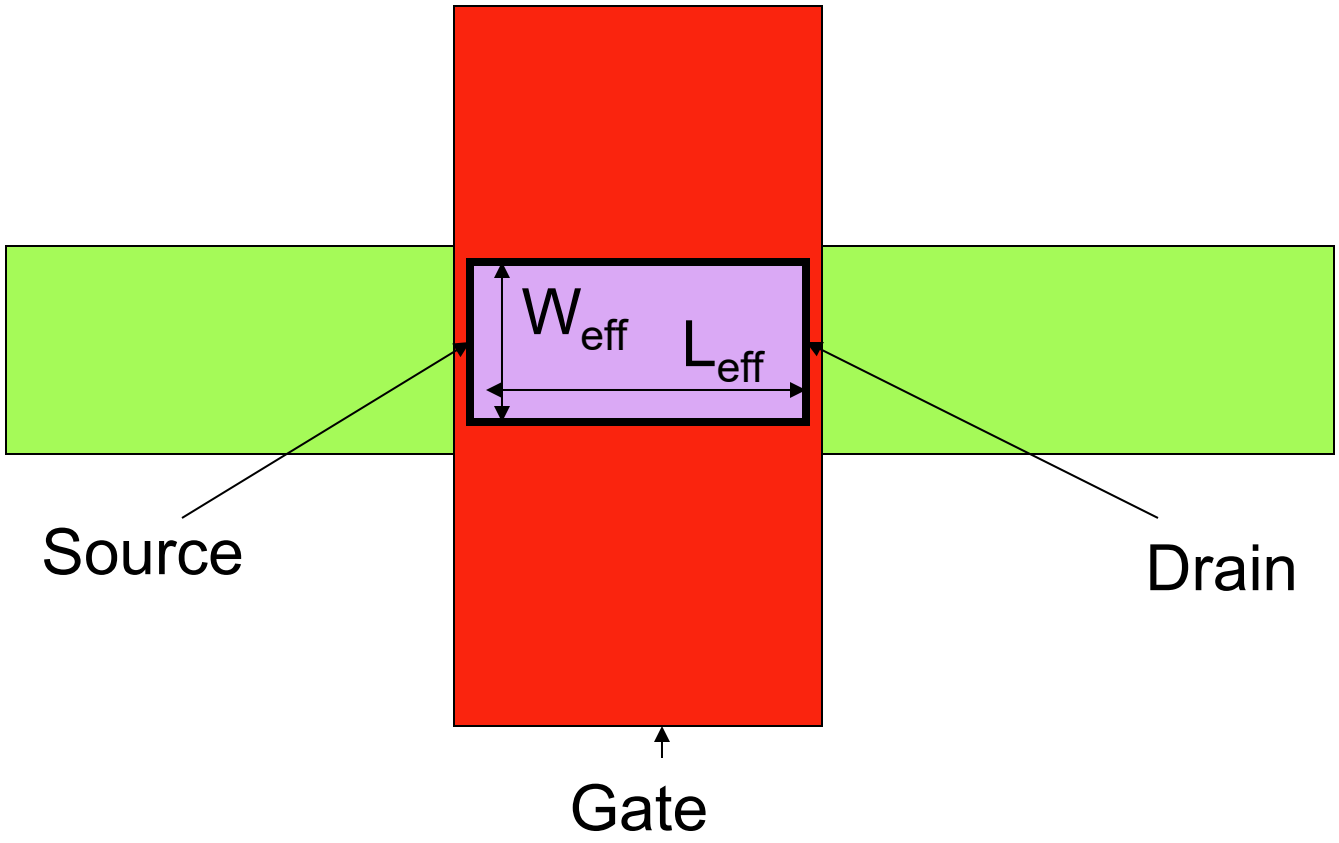
Henceforth, will assume planar devices unless specified to the contrary

MOS Transistor



Actual Drain and Source at Edges of Channel

MOS Transistor



Effective Width and Length Generally Smaller than Drawn Width and Length

Device and Die Costs

Characterize the high-volume incremental costs of manufacturing integrated circuits

Example: Assume manufacturing cost of an 8" wafer in a 0.25μ process is $800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

$$n_{trans} \cong \frac{A_{wafer}}{A_{trans}} = \frac{\pi(4in)^2}{(0.25\mu)^2} = 5.2E11$$

(520 Billion!)

(Trillion, Tera …10^{12})

$$C_{trans} = \frac{C_{wafer}}{n_{trans}} = \frac{\$800}{5.2E11} = \$15.4E-9$$

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!

Device and Die Costs

At $800/8” wafer, it can be easily shown that:

$$C_{per\ unit\ area} \cong \$2.5 / cm^2$$

Example: If the die area of the 741 op amp is 1.8mm^2 (including bonding pads), determine the cost of the silicon needed to fabricate this op amp

$$C_{741} = \$2.5 / cm^2 \bullet \left(1.8mm^2\right) \cong \$.05$$

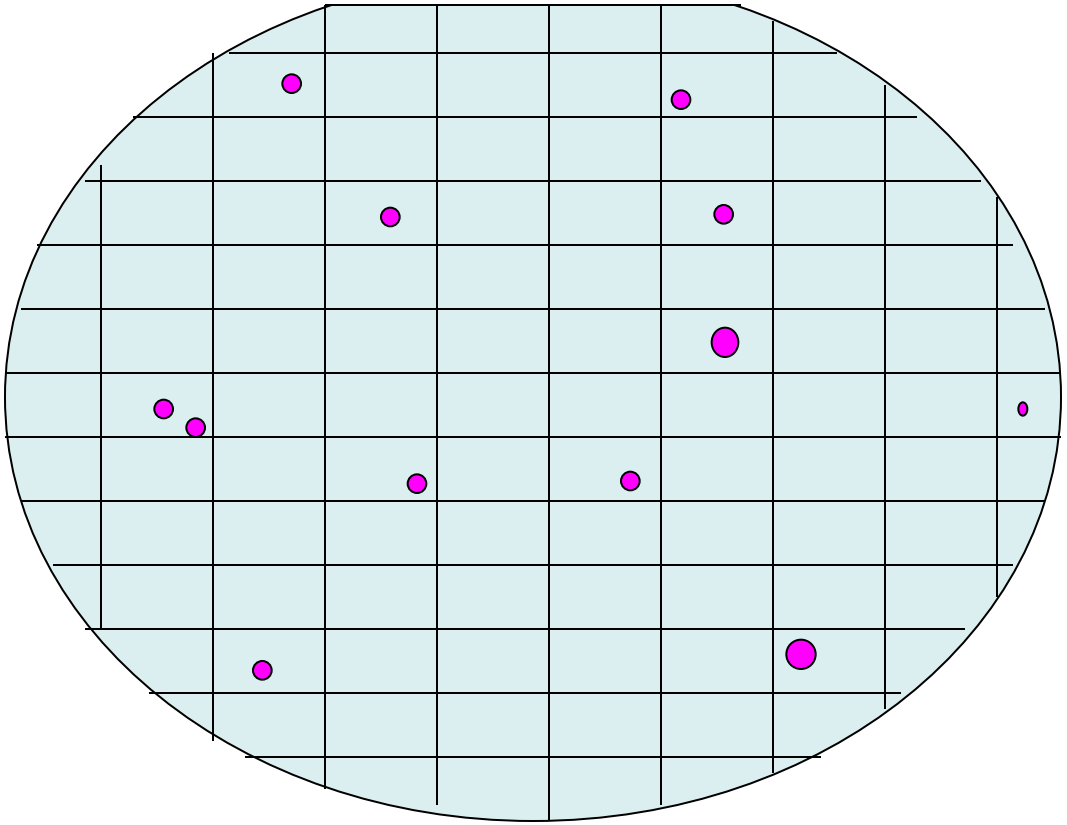
Actual integrated op amp will be dramatically less if bonding pads are not needed

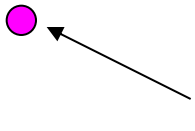
Physical Characteristics of Key Semiconductor Materials

Silicon:	Average Atom Spacing	$2.7\,\mathring{A}$
	Lattice Constant	$5.4\,\mathring{A}$
S_iO_2	Average Atom Spacing	$3.5\,\mathring{A}$
	Breakdown Voltage	$5 \text{ to } 10\text{MV/cm} = 5 \text{ to } 10\text{mV/}\mathring{A}$
Air		20KV/cm

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches

Defects in a Wafer





- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss

Yield Issues and Models

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed **Hard Faults**
- This is the major factor limiting the size of die in integrated circuits
- Wafer scale integration has been a “gleam in the eye” of designers for 3 decades but the defect problem continues to limit the viability of such approaches
- Several different models have been proposed to model the hard faults

Yield Issues and Models

- Parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)
- The circuits failures associated with these parametric variations are termed **Soft Faults**
- Increases in area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults

Hard Fault Model

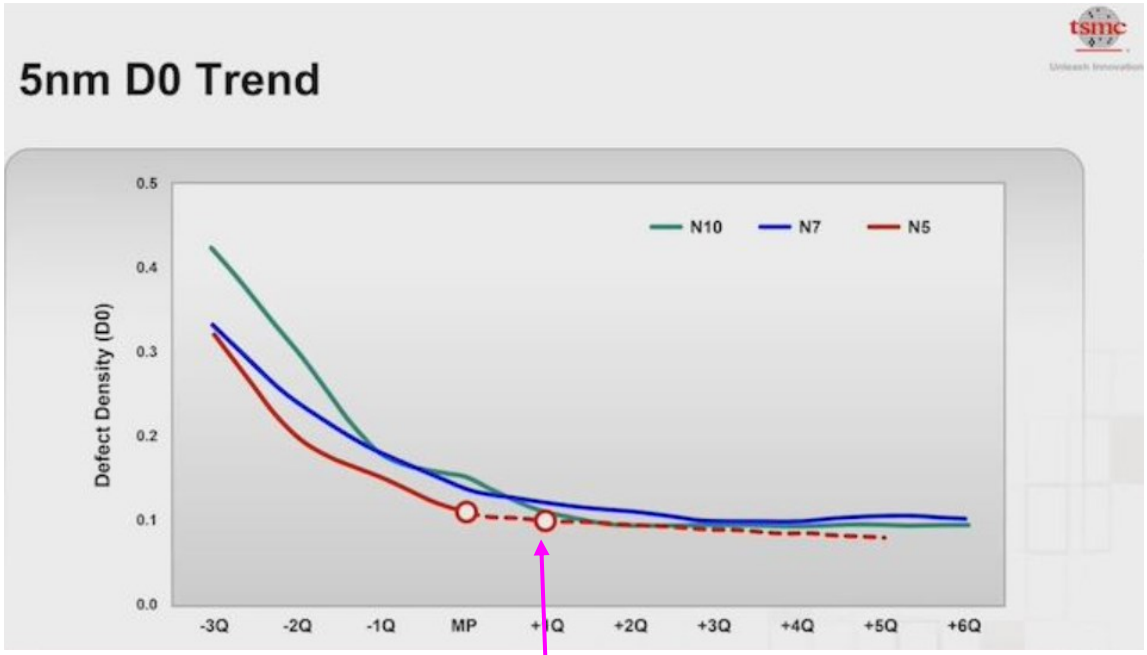
$$Y_H = e^{-Ad}$$

Y_H is the probability that the die does not have a hard fault
A is the die area
d is the defect density
(for some older processes, typically $1cm^{-2} < d < 2cm^{-2}$)
for some newer processes, typically $0.1cm^{-2} < d < 1cm^{-2}$)

Industry often closely guards the value of d for their process

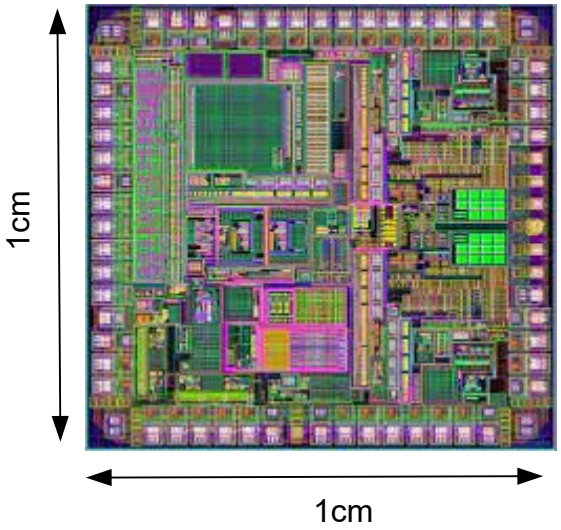
Other models, which may be better, have the same general functional form

Some processes have d under $0.1cm^{-2}$



- Aug 2020 article
- Defect density in per cm^2
- Smaller processes even have better defect density!!
- Note continued reduction predicted as process matures

Example:



Determine the hard yield of a die of area $1cm^2$ if the defect density is $1.5cm^{-2}$

$$Y_H = e^{-Ad}$$

$A=1cm^2$
$d=1.5cm^{-2}$

$$Y_H = e^{-1 \bullet 1.5} = 0.22$$

How good must the defect density be if we must obtain a 95% yield for the $1cm^2$ die?

$A=1cm^2$
$Y_H=0.95$

$$0.95 = e^{-1 \bullet d} \Longrightarrow d=-\ln(0.95) \Longrightarrow d=0.05cm^{-2}$$

Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

$$\sigma = \frac{\rho}{\sqrt{A_k}}$$

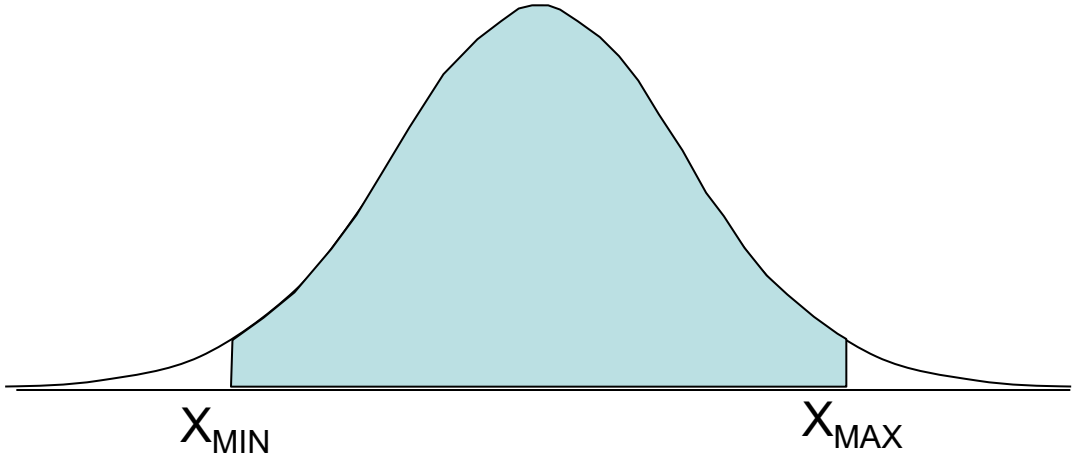
ρ is a constant dependent upon the architecture and the process

A_k is the area of the parameter sensitive area

Soft Fault Model

$$P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x)dx$$

P_{SOFT} is the soft fault yield
f(x) is the probability density function of the parameter of interest
X_{MIN} and X_{MAX} define the acceptable range of the parameter of interest



Some circuits may have several parameters that must meet performance requirements

Soft Fault Model

If there are k parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

$$Y_S = \prod_{j=1}^{k} P_{SOFT_j}$$

Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

$$Y = Y_H Y_S$$

Cost Per Good Die

The manufacturing costs per good die is given by

$$C_{Good} = \frac{C_{FabDie}}{Y}$$

where C_{FabDie} is the manufacturing costs of a fab die and Y is the yield

There are other costs that must ultimately be included such as testing costs, engineering costs, packaging costs, etc.

Example: Assume a die has no soft fault vulnerability, a die area of $1cm^2$ and a process has a defect density of $1.5cm^{-2}$

a) Determine the hard yield
b) Determine the manufacturing cost per good die if 8” wafers are used and if the cost of the wafers is $1200

Solution

a) $$Y_H = e^{-Ad}$$

$$Y = e^{-1\text{cm}^2 \bullet 1.5\text{cm}^{-2}} = 0.22$$

b) $$C_{Good} = \frac{C_{FabDie}}{Y}$$

$$C_{FabDie} = \frac{C_{Wafer}}{A_{Wafer}} A_{Die}$$

$$C_{FabDie} = \frac{\$1200}{\pi(4\text{in})^2} 1\text{cm}^2 = \$3.82$$

$$C_{Good} = \frac{\$3.82}{0.22} = \$17.37$$

Stay Safe and Stay Healthy !

End of Lecture 3